

Patents Citing Our Academic Work / Patentes que Citan Nuestros Trabajos Académicos

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Six of our papers published in conferences and journals have been cited by **21 patents and patent applications** from the companies **IBM, ARM, Qualcomm, AMD, Synopsys, Google, and Ddaim**.

Seis de nuestros artículos publicados en congresos y revistas han sido citados por **21 patentes y solicitudes de patente** pertenecientes a las empresas **IBM, ARM, Qualcomm, AMD, Synopsys, Google y Ddaim**.

[1] Speculative Early Register Release

Jesús Alastruey, Teresa Monreal, Víctor Viñals, Mateo Valero. *3rd Conference on Computing Frontiers (CF'06)*, ACM, 2006. DOI: 10.1145/1128022.1128061

Cited by/Citado por:

- **Qualcomm** — *Use of Register Renaming System for Forwarding Intermediate Results Between Constituent Instructions of an Expanded Instruction*. US 7669039 B2 (2010-02-23). [Lens.org]

[2] Microarchitectural Support for Speculative Register Renaming

J. Alastruey, T. Monreal, V. Viñals, M. Valero. *IEEE International Parallel and Distributed Processing Symposium (IPDPS 2007)*.

Cited by/Citado por:

- **ARM** — *Tracking Speculative Execution of Instructions for a Register Renaming Data Store*. US 9361111 B2 (2016-06-07). [Lens.org]

- **ARM** — *Technique for Freeing Renamed Registers*. US 9400655 B2 (2016-07-26). [Lens.org]

- **IBM** — *Tracking Operand Liveness Information in a Computer System and Performing Function Based on the Liveness Information*. US 10078515 B2 (2018-09-18). [Lens.org]

- **Qualcomm** — *Freeing Physical Registers in a Microprocessor*. WO 2015/142435 A1 (2015-09-24). [Lens.org]

[3] Selection of the Register File Size and the Resource Allocation Policy on SMT Processors

Jesús Alastruey, F. J. Cazorla, T. Monreal, V. Viñals, M. Valero. *20th Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, Campo Grande, Brasil, 2008.

Cited by/Citado por:

- **IBM** — 12 related patents/ 12 patentes relacionadas. List at/Listado en IEEE Xplore → Citations → Patents

[4] Concertina: Squeezing in Cache Content to Operate at Near-Threshold Voltage

A. Ferrerón, D. Suárez-Gracia, J. Alastruey-Benedé, T. Monreal-Arnal, P. Ibáñez. **IEEE Transactions on Computers*, vol. 65, no. 3, pp. 755–769, March 2016.

DOI: 10.1109/TC.2015.2479585

Cited by/Citado por:

- **AMD** — *Method and Apparatus for Using Compression to Improve Performance of Low Voltage Caches*. US 10884940 B2 (2021-01-05). [Lens.org]

- **Synopsys** — *Memory Write Assist*. US 12243585 B1 (2025-03-04). [Lens.org]

[5] Berti: an Accurate Local-Delta Data Prefetcher

Agustín Navarro-Torres, Biswabandan Panda, J. Alastruey-Benedé, Pablo Ibáñez, Víctor Viñals-Yúfera, Alberto Ros. *55th ACM/IEEE International Symposium on Microarchitecture (MICRO 2022)*, October 1–5, 2022, Chicago, Illinois, USA, pp. 975-991.

Cited by/Citado por:

- **Google** — *Dynamic Distance Adjustment For Stride Prefetcher*. WO 2025/090058 A1 (2025-05-01). [Lens.org]

[6] Developing an AI IoT Application with Open Software on a RISC-V SoC

Enrique Torres-Sánchez, Jesús Alastruey-Benedé, Enrique Torres-Moreno. *XXXV Conference on Design of Circuits and Integrated Systems (DCIS 2020)*, Segovia, Spain, 2020, pp. 1–6.

Cited by/Citado por:

- **Ddaim** — *Modular SoC AI/ML inference engine with dynamic updates using a hub-and-spoke topology at each neural network layer*. US 12353987 B1 (2025-07-08). [Lens.org]

Summary/Resumen

Paper/Artículo	Citing companies	# of patents
[1] Speculative Early Register Release	Qualcomm	1
[2] Speculative Register Renaming	ARM, IBM, Qualcomm	4
[3] SMT Processors / Register File Policy	IBM	12
[4] Concertina	AMD, Synopsys	2
[5] Berti	Google	1
[6] AI IoT RISC-V	Ddaim	1
Total	7 companies/empresas	21 citing patents