



Escuela de
Ingeniería y Arquitectura
Universidad Zaragoza



Departamento de
Informática e Ingeniería
de Sistemas
Universidad Zaragoza



30237 Multiprocesadores

3^{er} curso, Grado en **Ingeniería Informática**
Especialidad en **Ingeniería de Computadores**
Curso 2022-23

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Docencia: 6 ECTS

■ Trabajo del estudiante, 150 horas:

- Clases magistrales: 30 horas
- Clases de problemas: 15 horas
- Clases de prácticas: 15 horas
- Trabajo 12 horas
- Estudio personal: 85 horas
- Evaluación: 5 horas

■ Horario de clase

- Teoría: Martes 16h-17h, Miércoles 14h-16h
- Prácticas (L0.03, L0.01): Lunes 11h-13h, 6-7 sesiones

■ Tutorías: mejor bajo demanda

Evaluación

La evaluación consta de tres partes, 100 puntos:

1. Examen: 60 puntos. Mínimo 4 sobre 10
 - Teoría, problemas
 2. Cuestiones sobre las prácticas de laboratorio: 20 puntos
 3. Resultados sobre trabajo práctico no presencial: 20 puntos
-
- Las notas obtenidas en cada parte en C1 se mantendrán para C2 del mismo curso, pero no para convocatorias de cursos distintos

Prácticas

- 6-7 sesiones de 2 horas en el **laboratorio L0.03 o 0.01**
 - **NO se entregan memorias**,
pero es necesario realizarlas para contestar en el examen
 - Se realiza una **evaluación** de cada práctica (cuestiones más relevantes)
 - 1 grupo: lunes 11h-13h
- Módulo I: **Vectorización x86**
 - 3 sesiones. Calendario tentativo: 13F, 27F, 13M
 - Arquitectura x86-64 con SO CentOS (PCs L0.03)
- Módulo II: Programación de computadores de memoria compartida con **OpenMP**
 - 3 sesiones, con los siguientes sistemas:
 - ◆ Arquitectura x86-64 con SO CentOS (PCs L0.01)
 - ◆ Arquitectura ARM (RISC) con SO CentOS (pilgor)

Trabajos dirigidos (optativo)

- Pueden subir nota
- Estamos abiertos a cualquier propuesta, individual o colectiva
- Ejemplos
 - Vectorización sobre otras arquitecturas: ARM Neon (pilgor)...
 - Medidas de energía y potencia en programas paralelos
 - Overclocking con refrigeración forzada y eficiencia energética

Programa

■ MÓDULO I (-1/2)

- Procesadores Vectoriales Segmentados
 - ◆ Supercomputadores “clásicos”
- Extensiones multimedia, Intel AVX

■ MÓDULO II (+1/2)

- Multiprocesadores Memoria Compartida
 - ◆ Chips multiprocesador (*multicore, CMPs*)

Destrezas, habilidades, competencias

- Claves del rendimiento de un computador paralelo
 - ↑ velocidad
 - ↓ memoria
 - ↓ energía
- Compra o venta de servidores de cálculo
 - **Vigilancia tecnológica**: saber evaluar una compra y presentar una oferta desde el punto de vista técnico
- Introducción a la investigación experimental
 - **Metodología experimental**: diseñar experimentos, medir tiempos y eventos (máquina real o simulador), analizar, diseñar mecanismos hw-sw para aumentar el rendimiento

Bibliografía

- [CSG98] D.E. CULLER, J.P. SINGH y A. GUPTA, [Parallel Computer Architecture: a Hardware/Software approach](#), Morgan Kaufmann, 1998.
- [DaTo04] W. DALLY and B. TOWLES, [Principles and Practices of Interconnection Networks](#), Morgan Kaufmann, 2004.
- [Baer09] Jean-Loup BAER, [Microprocessor architecture: from simple pipelines to chip multiprocessors](#). Cambridge University Press, 2009.
- [SHW11] D.J. SORIN, M.D. HILL, D.A. WOOD, [A primer on memory consistency and cache coherence. Synthesis Lectures on Computer Architecture](#), Morgan & Claypool Publishers, 2011.
- [DAS12] M. DUBOIS, M. ANNAVARAM, P. STENSTRÖM, [Parallel Computer Organization and Design](#), Cambridge University Press, 2012.
- [HePa12] J. HENNESSY and D. PATTERSON, [Computer Architecture: a quantitative approach](#). 5th Edition, Morgan Kaufmann, 2012.
 - Chapter 4. Data-Level Parallelism in Vector, SIMD, and GPU Architectures
 - Chapter 5. Thread-Level Parallelism
 - Online Appendices (<http://booksite.mkp.com/9780123838728/references.php>)
 - ◆ Appendix F: Interconnection Networks
 - ◆ Appendix G: Vector Processors in More Depth
 - ◆ Appendix I: Large-Scale Multiprocessors and Scientific Apps

Lecturas

■ Módulo I

- [HePa12]: Chapter 4, Appendix G, I

■ Módulo II

- [CSG98] caps. 1, 5, 6 y 8
- [DaTo04] cap. 1, 2, 3, 8, 12, 22
- [HePa12] cap. 5, Appendix I
- [DAS12] todo
- [SHW11] todo
- [Baer09] pp. 241-245 (IBM Power 4-5-6) y cap. 7

Otra información de interés

■ Sitio web de la asignatura

- Moodle
- <http://webdiis.unizar.es/~chus/docencia/mp/>
- <https://github.com/universidad-zaragoza/Multiprocesadores>

■ Material disponible

- Transparencias de clase
- Colecciones de problemas
- Enunciados de prácticas
- Lecturas

¡Un poco de motivación!



AMD EPYC™ 7742

AMD EPYC™ 7742

6,950\$ (precio salida)

# of CPU Cores: 64	# of Threads: 128	Base Clock: 2.25GHz
Max Boost Clock ⓘ: Up to 3.4GHz	Total L3 Cache: 256MB	Package: SP3
Socket Count: 1P/2P	PCI Express® Version ⓘ: PCIe 4.0 x128	Default TDP / TDP ⓘ: 225W
System Memory Specification ⓘ: 3200MHz	System Memory Type: DDR4	Memory Channels: 8
Per Socket Mem BW: 204.8 GB/s		

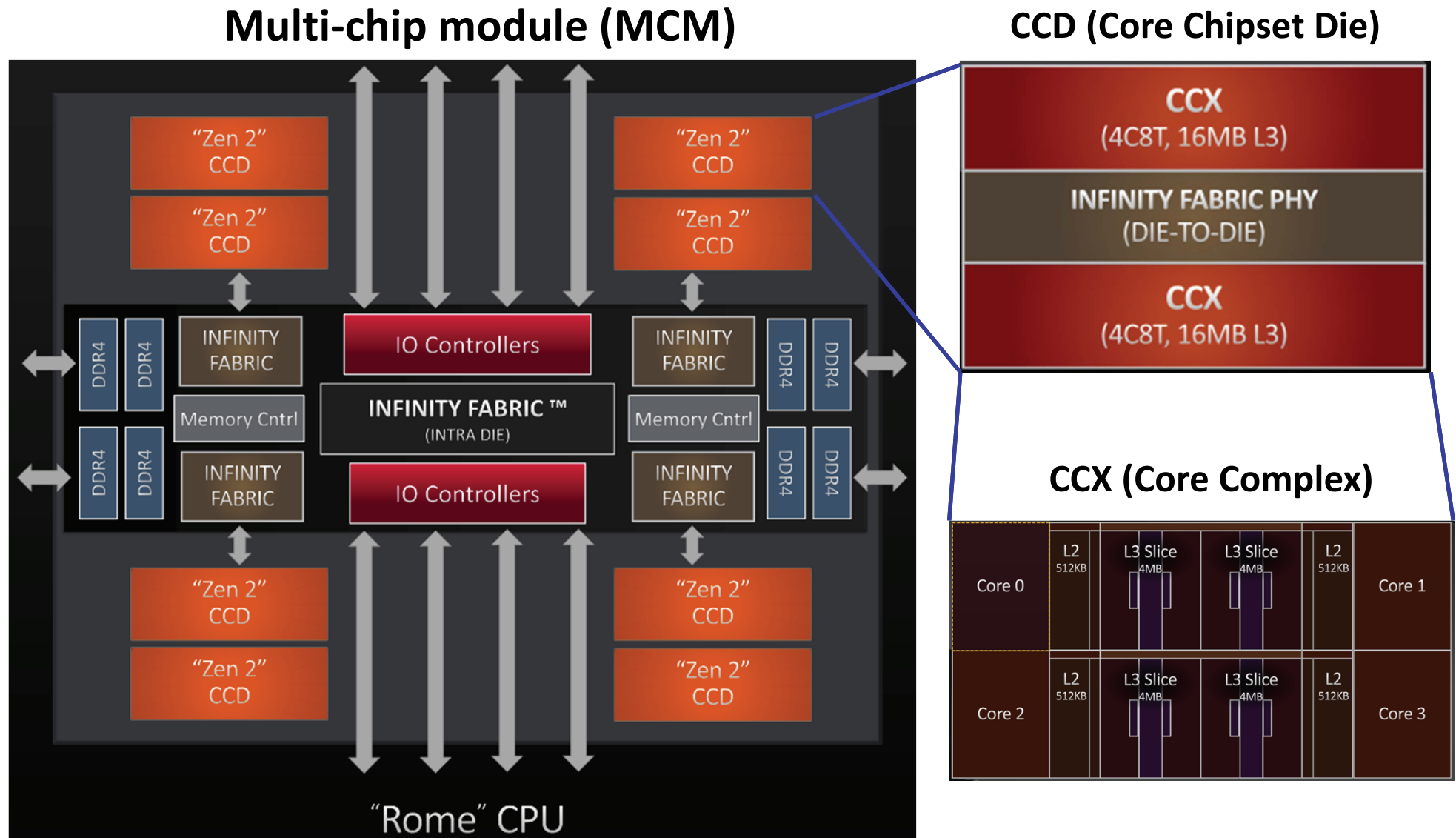
<https://www.amd.com/en/products/cpu/amd-epyc-7742>

AMD EPYC™ 7002 Series Processors

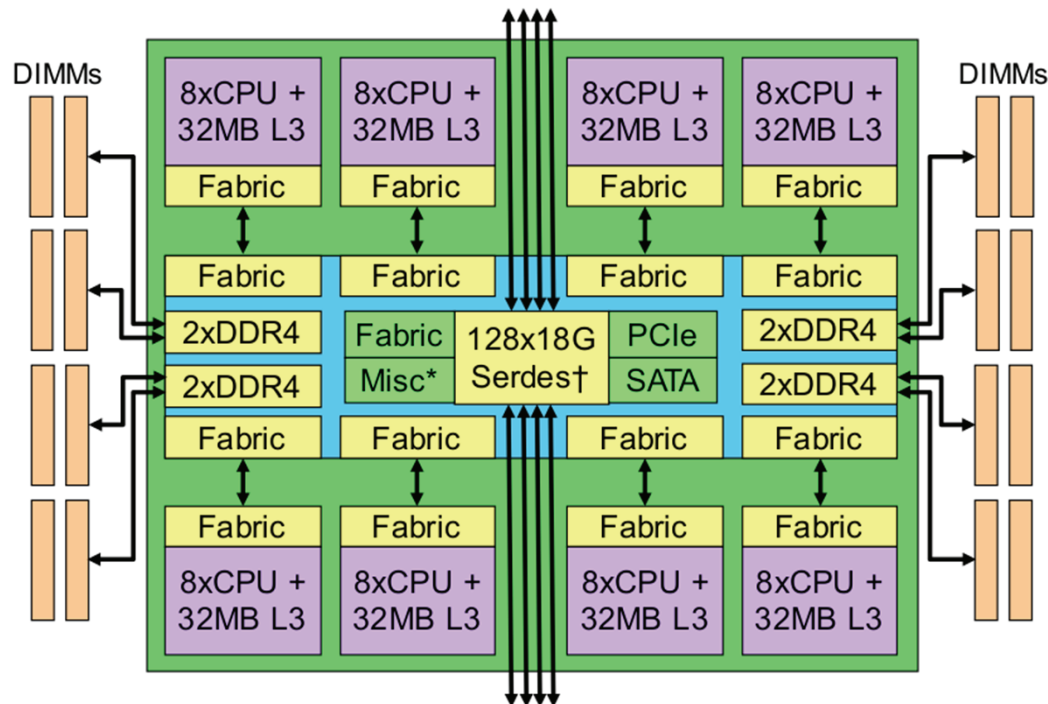
Model	Cores	Threads	Base Freq. (GHz)	Max. Boost Freq. (GHz) ^a	TDP (W)	L3 Cache (MB)	DDR Channels	Max DDR Freq. (1DPC) ^c	Per-Socket Theoretical Memory Bandwidth (GB/s)	PCIe® Gen 4 Lanes ^c	2P/1P
7742	64	128	2.25	3.40	225 ^c	256	8	3200	204.8	128	2P/1P
7702	64	128	2.00	3.35	200	256	8	3200	204.8	128	2P/1P
7702P											1P only
7642	48	96	2.30	3.30	225 ^c	256	8	3200	204.8	128	2P/1P
7552	48	96	2.20	3.30	200	192	8	3200	204.8	128	2P/1P
7542	32	64	2.90	3.40	225 ^c	128	8	3200	204.8	128	2P/1P

<https://www.amd.com/system/files/documents/AMD-EPYC-7002-Series-Datasheet.pdf>

AMD EPYC™ Processor (Rome)



AMD EPYC™ Processor (Rome)



Chip: hasta 8 CCDs (64 cores) conectados por ¿?

CCD: 8 cores/16 threads + 32 MiB L3

Memory: 8 canales DDR4-3200,
4 TiB (8 can. x 2 DIMMs/canal x 256GiB/DIMM)

I/O: 128 lanes PCIe Gen4

Fabric: Infinity Fabric

Vector Max Perf (R_{peak}): 2.3/4.6 TFLOPS DP/SP

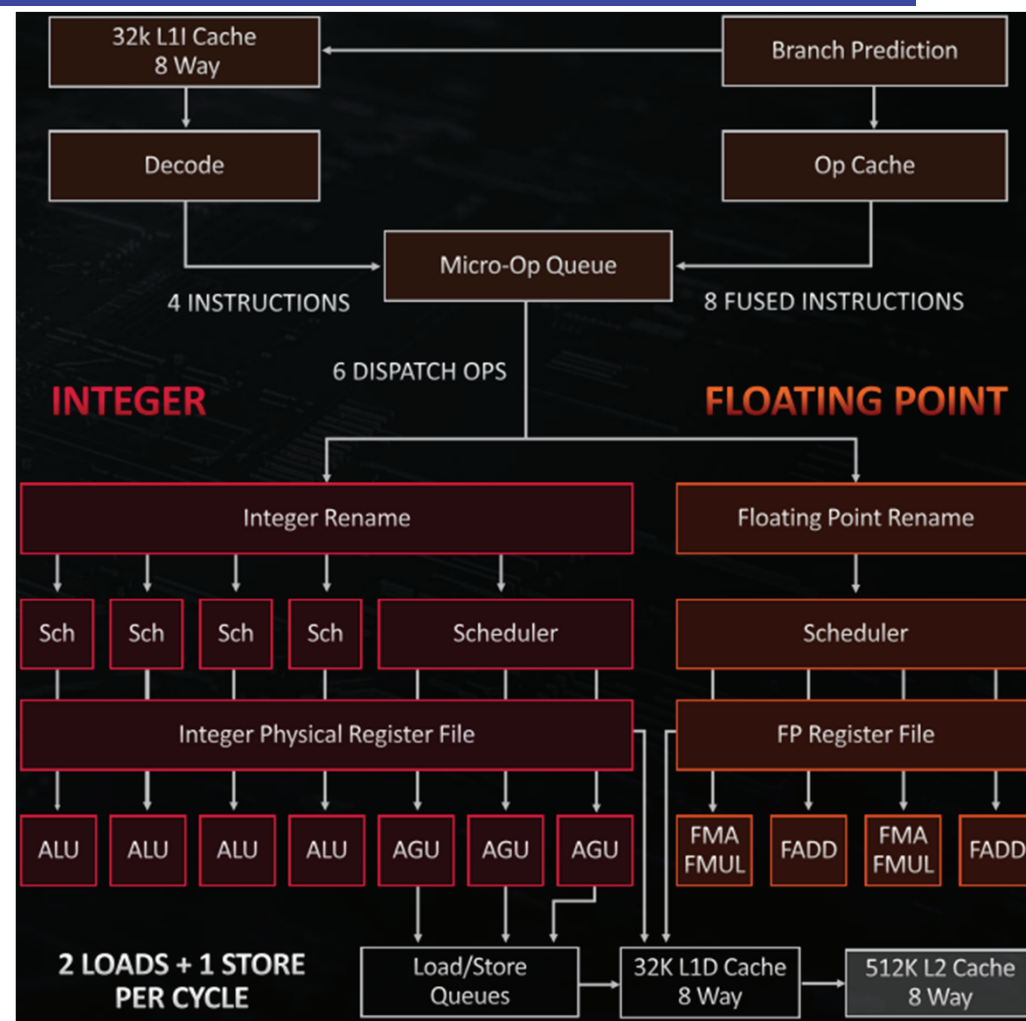
Stream Triad: ~200 GB/s

Figura: Linley Gwennap. AMD Rome Ruins Intel Hegemony. Microprocessor Report. Agosto 2019.

Resultados Stream: Review: AMD Epyc 7742 2P Rome Server: <https://hexus.net/tech/reviews/cpu/133244-amd-epyc-7742-2p-rome-server/?page=4>

AMD 2nd Gen EPYC™ Processor, Zen 2 (Rome)

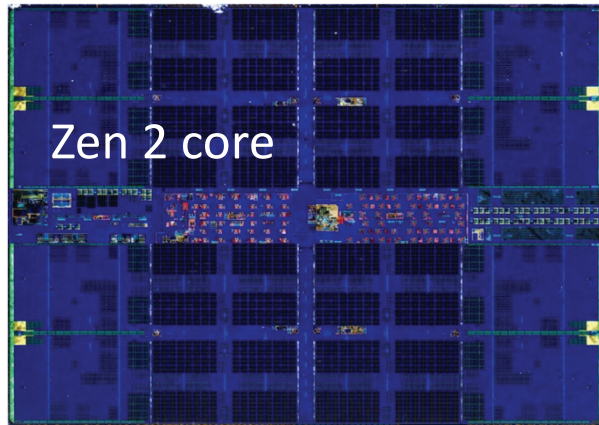
- X86-64 architecture
- 4K op cache
- Dispatch: 6 uops/cycle
- Issue: 7 + 4 uops/cycle (4 ALUs + 3 AGUs + 4 FPs)
- Integer RF: 180 x 64b
- Vector RF: 160x 256b
- 224-entry ROB
- 2 x FP data path width
- L1: 2 load + 1 store
- 2 threads per core



Zen 2 core

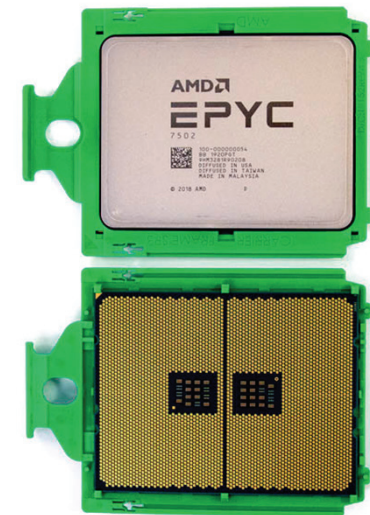
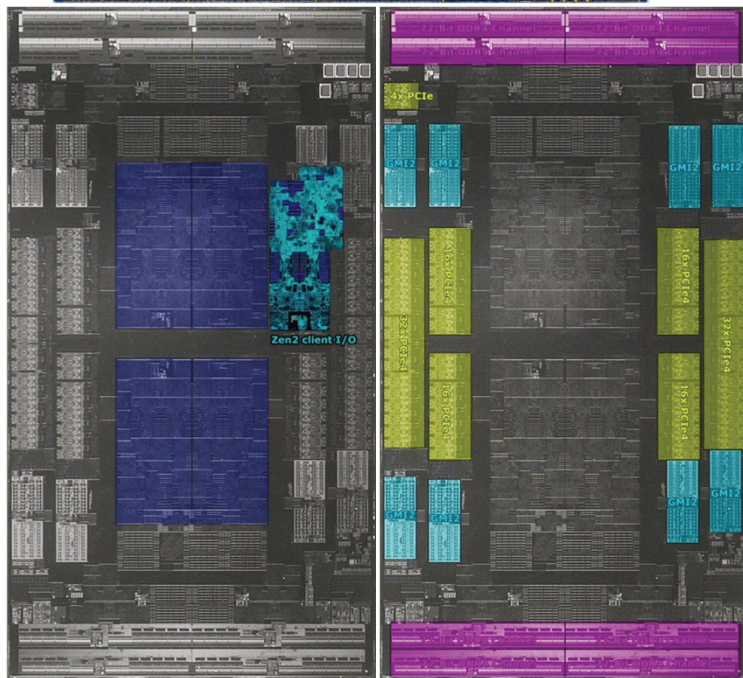
DP, sin FMA → 4 UFs x 4 ops/UF x 64 cores x 2.25 GHz = 2.3 TFLOPS
 DP, con FMA → XX
 SP, sin FMA → 4 UFs x 8 ops/UF x 64 cores x 2.25 GHz = 4.6 TFLOPS
 SP, con FMA → XX

AMD EPYC™ 7742: Packaging

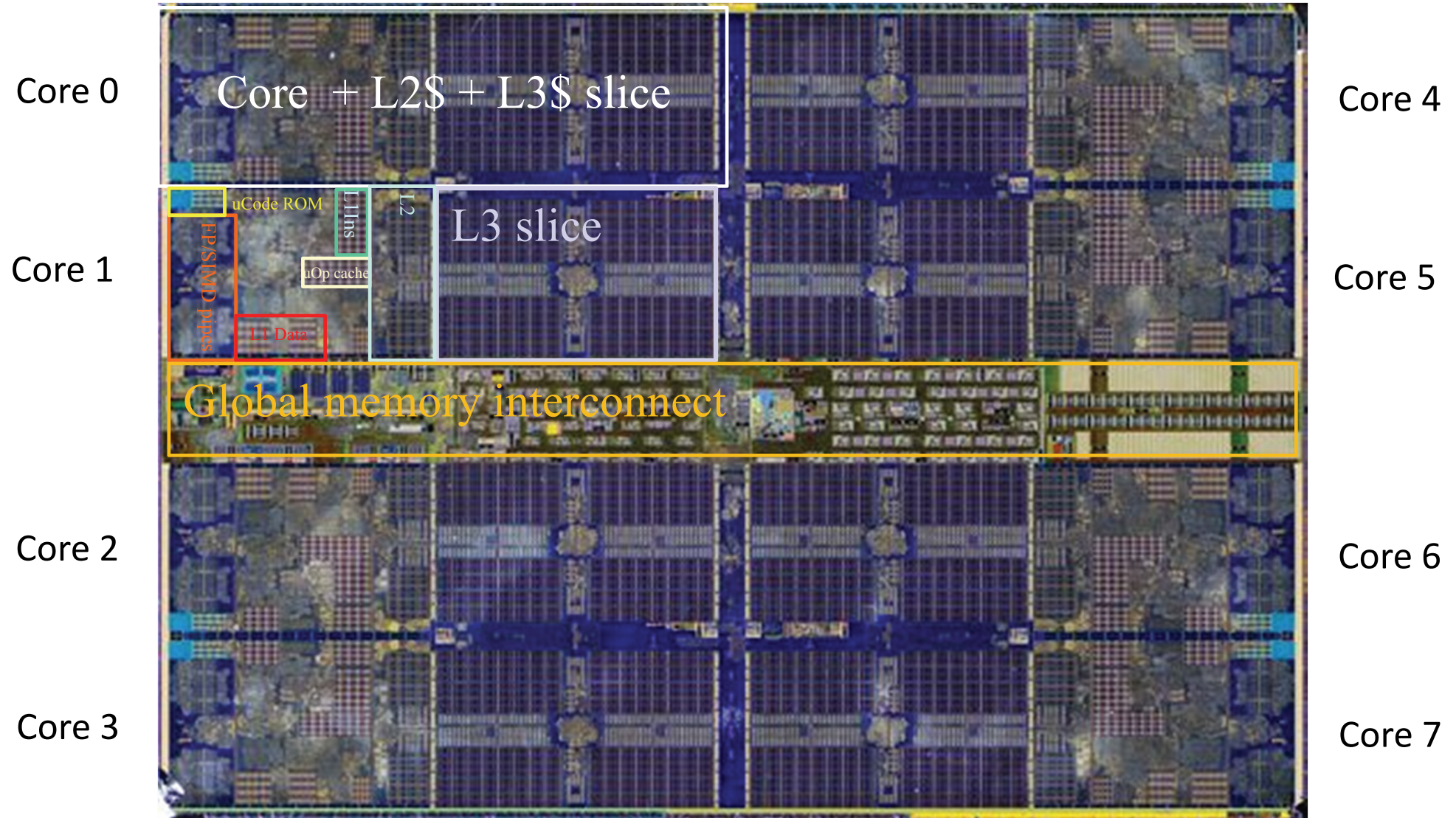


World population is expected to reach 8 billion people in 2023 according to the United Nations (in 2026 according to the U.S. Census Bureau)

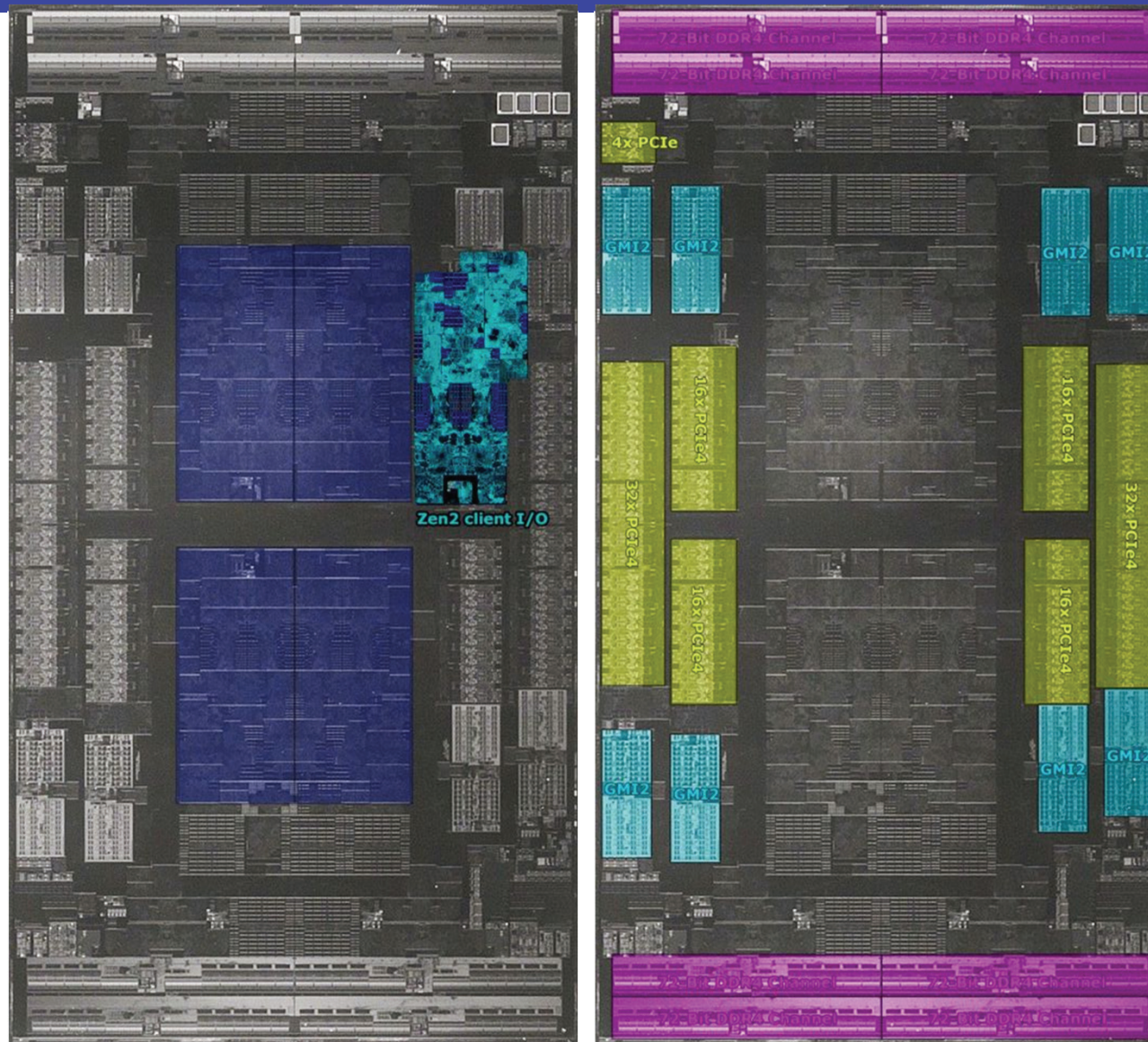
Package	FCLGA-4094 (LGA)
Dimension	58.5 mm × 75.4 mm
Pitch	1.00 mm
Contacts	4094
Socket	Socket SP3, LGA-4094
#transistor	39.53 billion (american)
IOD #trans	8.34 billion (american)
IOD area	416mm ²
Zen2 area	74 mm ²



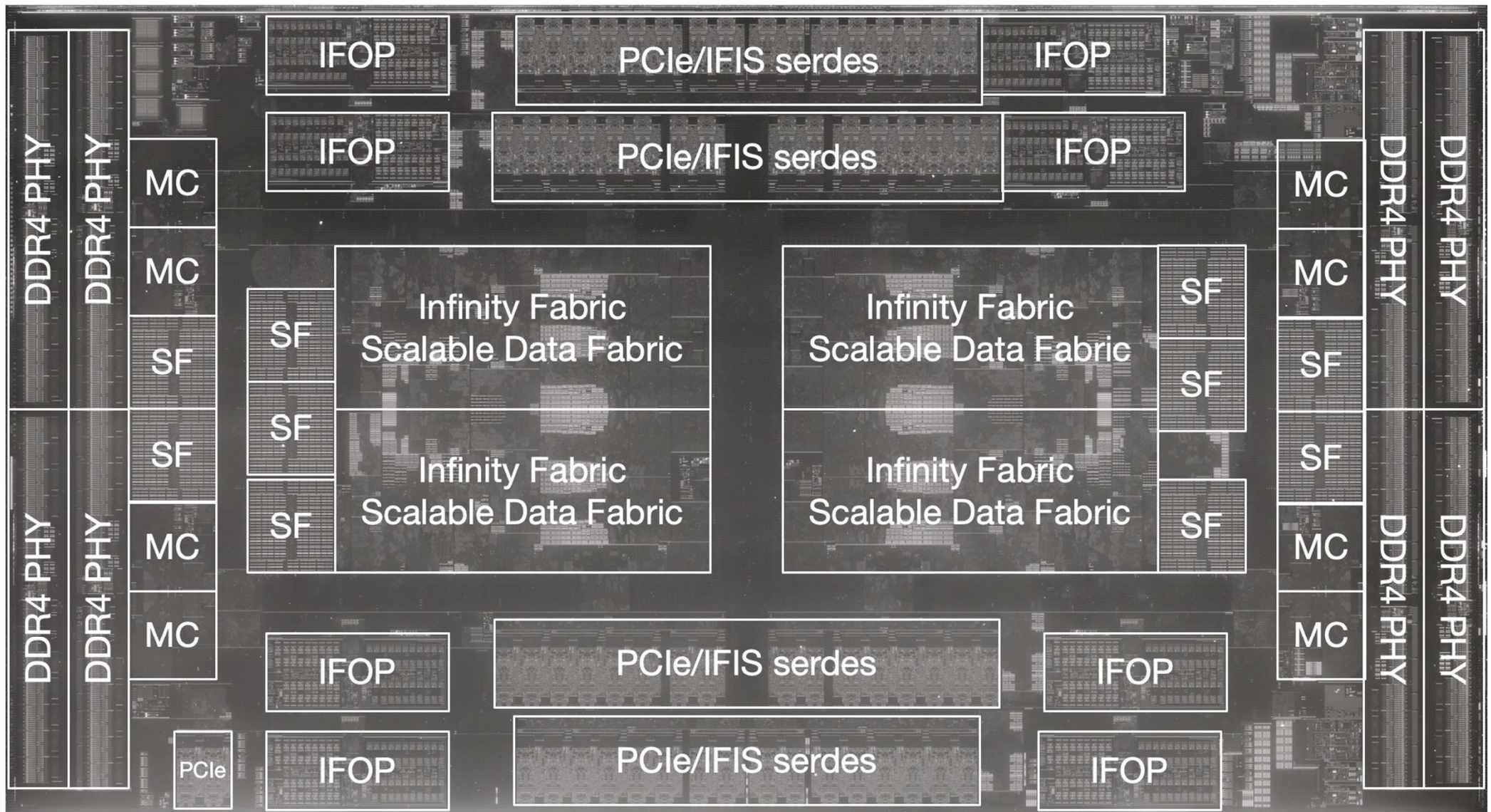
AMD EPYC™ 7742: Zen2 in detail



AMD EPYC™ 7742: IOD in detail



AMD Zen 2 Rome Server IO Die (sIOD)



IFOP: Infinity Fabric On Package aka GMI2, IFIS: Infinity Fabric Inter-Socket, MC: memory controller?, SF: snoop filter/coherence directory?
 Die photo by Fritzchens Fritz <https://www.flickr.com/photos/130561288@N04/48949317691/> annotation by Wes Felter @wmf v1 24 Oct 2019

Servidores Altas Prestaciones

- Supermicro

- <https://www.thinkmate.com/systems/supermicro/ultraserver>



Heterogeneous Multicore Chips



Beginning Fall 2021

Alder Lake

Reinventing Multi Core Architecture

Single, Scalable SoC Architecture

All Client Segments – 9W to 125W – built on Intel 7 process

All-New Core Design

Performance Hybrid with Intel Thread Director

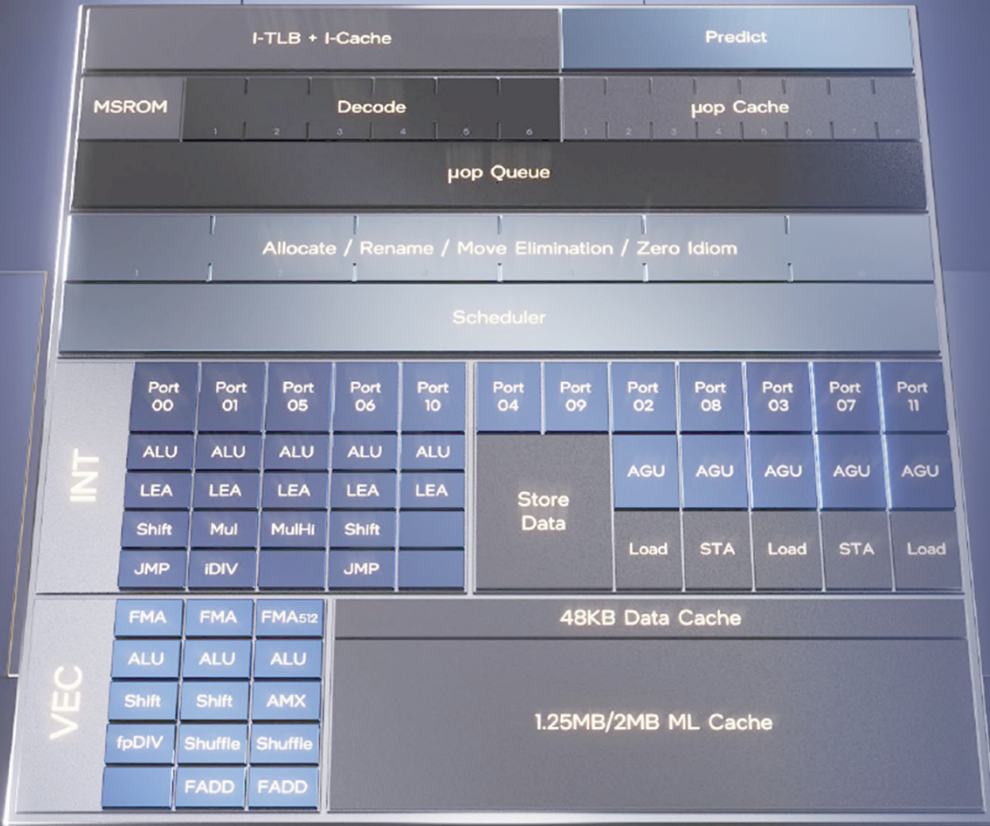
Industry-Leading Memory & I/O

DDR5, PCIe Gen5, Thunderbolt™ 4, Wi-Fi 6E

Some of them for efficiency



Some of them for high performance



The diagram illustrates the internal architecture of an Intel x86 Core. It is organized into several functional blocks:

- Top Section:** Includes the I-TLB + I-Cache, Predict, MSROM, Decode (with sub-units 1-6), and µop Cache (with sub-units 1-7).
- µop Queue:** A central queue for micro-operations.
- Allocate / Rename / Move Elimination / Zero Idiom:** A block for instruction optimization.
- Scheduler:** Manages the execution flow.
- INT (Integer) Section:** Contains 12 ports (Port 00-11). Ports 00-03, 05-06, and 09-10 are connected to ALU, LEA, Shift, Mul, MulHi, and JMP units. Ports 04 and 08 are connected to a Store Data unit. Ports 02, 07, and 11 are connected to AGU, Load, and STA units.
- VEC (Vector) Section:** Contains FMA, FMA512, ALU, Shift, AMX, fpDIV, Shuffle, and FADD units.
- Caches:** A 48KB Data Cache and a 1.25MB/2MB ML Cache.

New Performance x86 Core
A Step Function in CPU Architecture
Performance For the Next Decade of Compute

A significant IPC boost at high power efficiency

Wider Deeper Smarter

- Better supports large data set and large code footprint applications
- Enhanced power management improves frequency and power
- Machine Learning Technology: Intel® AMX – Tile Multiplication

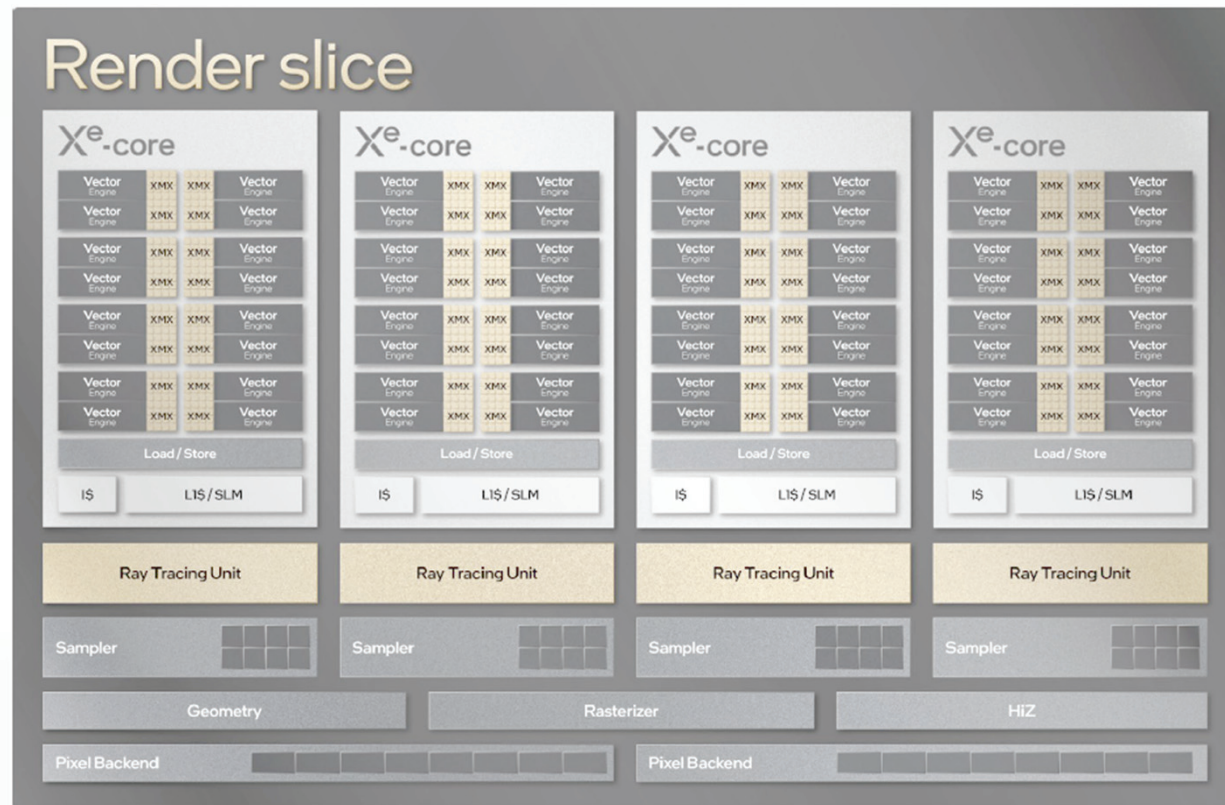
All in a tailored scalable architecture to serve the full range of Laptops to Desktops to Data Centers

Architecture Day 2021  50

Some of them for specific purpose



Render Slice



General overview. Also P and U - series

	Processor Number	Processor Cores	Processor Threads	Performance Cores	Efficient Cores	L3 Cache	Max Turbo Frequency P-cores	Max Turbo Frequency E-cores	Base Frequency P-cores	Base Frequency E-cores	Processor Graphics	Max Graphics Frequency	Processor Base Power	Max Turbo Power	Intel vPro®
Intel CORE i9	i9-12900HK	14C	20T	6P	8E	24MB	5.0 GHz	3.8 GHz	2.5 GHz	1.8 GHz	96 EU	1.45 GHz	45W	115W	Essentials
	i9-12900H	14C	20T	6P	8E	24MB	5.0 GHz	3.8 GHz	2.5 GHz	1.8 GHz	96 EU	1.45 GHz	45W	115W	Enterprise
Intel CORE i7	i7-12800H	14C	20T	6P	8E	24MB	4.8 GHz	3.7 GHz	2.4 GHz	1.8 GHz	96 EU	1.4 GHz	45W	115W	Enterprise
	i7-12700H	14C	20T	6P	8E	24MB	4.7 GHz	3.5 GHz	2.3 GHz	1.7 GHz	96 EU	1.4 GHz	45W	115W	Essentials
	i7-12650H	10C	16T	6P	4E	24MB	4.7 GHz	3.5 GHz	2.3 GHz	1.7 GHz	64 EU	1.4 GHz	45W	115W	-
Intel CORE i5	i5-12600H	12C	16T	4P	8E	18MB	4.5 GHz	3.3 GHz	2.7 GHz	2.0 GHz	80 EU	1.4 GHz	45W	95W	Enterprise
	i5-12500H	12C	16T	4P	8E	18MB	4.5 GHz	3.3 GHz	2.5 GHz	1.8 GHz	80 EU	1.3 GHz	45W	95W	Essentials
	i5-12450H	8C	12T	4P	4E	12MB	4.4 GHz	3.3 GHz	2.0 GHz	1.5 GHz	48 EU	1.2 GHz	45W	95W	-

Intel® processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. The frequency of cores and core types varies by workload, power consumption and other factors. Visit <https://www.intel.com/content/www/us/en/architecture-and-technology/turbo-boost/turbo-boost-technology.html> for more information. i9-12900HK supports CPU Over Clocking. Memory Ratio Override is not supported. Intel Thermal Velocity Boost not supported on 12th Gen mobile processors; Max Turbo Frequency for P-cores may include Intel Turbo Boost Max 3.0. All SKUs support up to DDR5 (4800 MT/s)/DDR4 (3200 MT/s)/LPDDR5 (5200 MT/s)/LPDDR4 (4267 MT/s) memory. See ark.intel.com for more specification details.

Embargoed until January 4, 2022, at 10:10 AM PT

Ejercicio 1: Simulando y cocinando con el EPYC 7742

- Vitro LG KA60530A: **2.3kW** en $3.14 \times 110^2 = 38013.36 \text{ mm}^2$
- AMD EPYC 7742: W en mm^2

- Caben unos
- Disiparía
- Max FLOP/ciclo ?
 - ◆ Sin multiply/add
 - ◆ Con multiply/add
- Tiempo simulaciones aerodinámicas *sin* FMA:
 - ◆ Ala estacionaria 10^{18}
 - ◆ Ala turbulenta 10^{20}
 - ◆ Avión turbulento 10^{23}
- Coste simulaciones ? (0.17 €/KWh)

