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José Luis Briz – Short Bio

José Luis Briz is a tenured Associate Professor with the Department of Computer and Systems Engineering at the UZ. His research interests include memory hierarchy and processor microarchitecture, with a recent involvement in thermal-aware real-time scheduling on MPSoCs. He does also collaborate in embedded systems projects with the industry. Briz has a combined BS/MS degree in Geology, a MS degree in Computer Science, and a PhD in Computer Engineering, all of them from UZ, having published meaningful contributions to the application of computing to Structural Geology. He is a member of the gaZ group, the I3A Research Institute, and Affiliate of the HiPEAC European Network of Excellence. He is also a member of the ACM, the IEEE (Computer Society), the ISOC and of the Spanish Society of Computer Architecture (SARTECO). For a number of oddities, José Luis Briz belongs to the little History of the Internet (Who Is Who in the Internet World).

Current research

- Thermal-aware, energy efficient real-time scheduling on multiprocessor systems on chip (MPSoCs).

Research and academic summary

I started my research activities with a PhD dissertation at the UZ related to the implementation of Petri Nets, inside the field of Discrete Event Systems, proposing Linear Enabling Functions (LEFs), a fast way to characterize transition firing, which was extensively leveraged, with a side contribution on the modelling of a pipelined architecture. I then joined the Computer Architecture Group of the Univ. of Zaragoza (gaZ), where I started contributing in hardware data prefetching techniques, co-advising a PhD student, with results that led to the Best Paper Award in the 1st. Data Prefetching Championship, held by Intel in Raleigh, NC, USA, 2009. For the last few years, I have been collaborating with the MASC Lab (UCSC, CA USA) on memory hierarchy optimizations for GPGPUs, also exploiting Voltage Stacking techniques for Near-Threshold Computing (NTC). This has resulted in a number of quality papers (ISLPED 2013, TACO 2016, IEEE TVLSI 2018), co-advising a PhD student at the Univ. of California Santa Cruz.

I am currently collaborating with the Advanced Research Center (CINVESTAV) in Guadalajara, Mexico, related to thermal-aware real-time scheduling in MPSoCs, targeting the accomplishment of time, thermal and energy constraints while reducing size, weight and power in aerospace, satellite and automotive embedded systems. I have supervised the PhD. Thesis of Gaddiel Desirena, and I am the current co-advisor of the PhD student Laura Rubio. We have so far achieved promising results presented and published in WODES 2016, WODES 2018, WODES20, TECS 2019, DEDS 2019 and IEEE Access. I also keep collaborating in other research lines of the gaZ associated to performance evaluation, efficient software and hardware implementation of algorithms and heuristics employed in Artificial Intelligence (vid. e.g. IEEE T-G 2017).

I have been collaborating with companies for a long time, mostly solving complex specific problems related to Linux security, poor system performance, or deadline misses in hard real-time systems. In most cases, I have often counted on senior undergrads, MSc or PhD students who have seamlessly joined the company or jumped to others related to the field. I have led formal and informal agreements with

international companies like Infineon and Intel Mobile Systems (Munich, Germany), ARM (Cambridge, UK) or BSH Spain (Zaragoza), besides a number of smaller local companies that benefit from this type of collaboration.

Part of my research has been related to multidisciplinary project in Geology – Geophysics and Computing, where I envisioned and developed two successful approaches based on laboratory and mathematical models, which complemented the initial single research avenue based on natural models, allowing the validation of restitution methods used for gas, oil and CO2 natural reservoir exploration. This work led to four articles in renowned journals. I also co-advised an MSc and PhD student. Her MSc thesis was awarded with the Premio García Siñériz to the best MSc contribution in Geophysics in Latin-America and Spain, and a Midland Valley Award.

I have been teaching courses on Computer Architecture, Operating Systems and Embedded Systems since 1994, at both the undergrad and MSc level, always at the UZ. I was a member of the Executive Board (Consejo de Gobierno) and Senate (Claustro) of the institution, and held the Vice-Chair position of my Department from 2012 to 2016.

Top 10 recent Publications

- Rubio-Anguiano, Laura, Chils-Trabanco, Abel, Briz J.L., Ramírez-Treviño, Antonio - Maximizing utilization and minimizing migration in thermal-aware energy-effcient real-time multiprocessor scheduling. IEEE Access. Online ISSN: 2169-3536 - Print ISSN: 2169-3536 - To appear. Early access on line. DOI: https://doi.org/10.1109/ACCESS.2021.3086698
- Rubio-Anguiano, L., Desirena-López, G., Ramírez-Treviño, A. et al. Energy-Efficient Thermal-Aware Multiprocessor Scheduling for Real-Time Tasks Using TCPN. Discrete Event Dynamic Systems (2019) 29 (3): 237-264. Sept. 2019 https://doi.org/10.1007/s10626-019-00285-x
- G. Desirena, A. Ramírez, J.L. Briz, C.R. Vázquez, D. Gómez. Thermal-Aware Real-Time Task Scheduling in MPSoCs using Timed Continuous Petri Nets. ACM Trans. Embed. Comput. Syst. 18, 4, 16 Article 36 (May 2019), 24 pages. 17 https://doi.org/10.1145/3322643
- R. Trapani, E. Ebrahimi, E. Ardestani, A. Sankaranarayanan, J. L. Briz, J. Renau - GPU NTC Process Variation Compensation with Voltage Stacking - IEEE Transactions on VLSI (26) 9, Sept. 2018 pp: 1713 - 1726. DOI: 10.1109/TVLSI.2018.2831665
- J. Olivito, J. Resano and J. L. Briz, "Accelerating Board Games Through Hardware/Software Codesign," in IEEE Transactions on Computational Intelligence and AI in Games, vol. 9, no. 4, pp. 393-401, Dec. 2017. doi: 10.1109/TCIAIG.2016.2604923
- L. Rubio, G. Desirena, A. Ramírez-, J.L. Briz. Energy-Efficient Thermal-Aware Scheduling for RT Tasks Using TCPN. WODES'18, Castellammare di Stabia , Italy 2018.
- Desirena, G; Briz, J.L; Vazquez, C.R.; Ramirez, A; Gómez; D. On-line Scheduling in Multiprocessor Systems based on continuous control using Timed Continuous Petri Nets 13th WODES 2016 Xi'an, China May 30– June 1, 2016, DOI=10.1109/WODES.2016.7497860 ISBN: 978-1-5090-4190-9
- Ardestani, Ehsan K.; et al. 2016. Managing mismatches in voltage stacking with core unfolding. ACM TACO. 12-4, pp.43-68. ISSN 1544-3566.
- Ramón, M. J.; et al. 2015. Parametric unfolding of flexural folds using paleomagnetic vectors. GEOLOGICAL SOCIETY SPECIAL PUBLICATIONS. 425. ISSN 0305-8719..
- Sankaranarayanan, A.; et al.. An energy efficient GPGPU memory hierarchy with tiny incoherent caches. ISLPED 2013. pp. 9-14. ISSN 1533-4678.

Quality Metrics

- Research qualified periods (sexenios): 2
- Number of PhD thesis supervised for the last 10 yrs.: 3
- Total number of references: 30 (WoS) / 61 (Scopus) / 248 (Google Scholar)
- H index. 4 (de 27 publ. en WoS) / 5 (de 16 en Scopus) / 9 (de 35 publ. en Google Scholar)

Journals in Q1/Q2

- IEEE Access JCR Q1
- IEEE Transactions on VLSI 2018 (JCR Q2 impact factor 2018 1.946)
- Journal on Discrete Event Dynamic Systems (DEDS) (JCR 2018 Q2 impact factor 1.128)
- ACM Transactions on Architecture and Compilers (TACO) 2016 (JCR Q2 impact factor 1.636)
- Tectonophysics 2013 (JCR Q1 impact factor 2.866)
    - Mathematical Geosciences 2016 (JCR Q1 impact factor 1.653)
- Journal of Structural Geology 2012 (JCR Q2 impact factor 2.288)
- IEEE Micro 2006 (JCR Q1 impact factor 1.238)

References in patents

- JILP 2011 (Art. 8 en C.1.) Citado en US 9201798 B2. Dec 1, 2015 (IBM)
- Ramos, L.M, Briz, J.L., Ibáñez, P. and Viñals. Data prefetching in a cache hierarchy with high bandwidth and capacity. In Procs of MEmory performance: DEaling with Applications, systems and architectures (MEDEA '06). ACM, New York, NY, USA, 37-44. http://doi.acm.org/10.1145/1166133.1166138. Citada en US 7925865 B2 (Sun Microsystems Inc (May 30 2008), Oracle America Inc (Feb 12 2010)
- M. J. Garzarán, Briz, J.L., P.E. Ibáñez y Viñals, V. Pattern Characterization and Hardware Prefetching with Load Caches in Bus-Based Multiprocessors. 9th Euromicro Workshop on Parallel and Distributed Processing. Mantova (Italia) 8-9 Feb. 2001. Citada en US 7237068 (Sun Microsystems, Inc. 2007)

Please refer to http://webdiis.unizar.es/~briz/ *for a full list of papers and CV*