A SWN model for a multiprocessor architecture

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1 Introduction

The model, presented in this section, represents a multiprocessor architecture composed of a set of processors with their memories connected through a bus. Each processor p_i is associated with a local memory composed of two sections:

- **private (PM_i)**, it can be accessed only by the corresponding processor p_i through its private bus(PB);
- **common (CM_i)**, it can be accessed by all the processors in the system through a global bus (GB).

An access to the common memory module CM_i is performed by processor p_i through its local bus (LB), while processor p_j, $j \neq i$ needs global bus GB, and the local bus of P_i. Contention arises from the use of GB as well as of the local busses and CM modules. External access requests to CM modules have *priority* over the local CM accesses and causes their *preemption*.

The behavior of the system can be described as follows: a processor alternates periods of processing, requiring only access to the private memory, with periods of CM module accesses. Hence a processor p_i may be in one of the following states:

- **active**, the processor is executing in its private memory;
- **accessing local** CM_i, the processor is performing a local CM_i module access;
- **accessing remote** CM_j, the processor is performing a CM_j module access;
- **queued**, the processor is waiting for the GB to become available;
- **blocked**, the processor is waiting to continue a local CM access preempted by an external access.

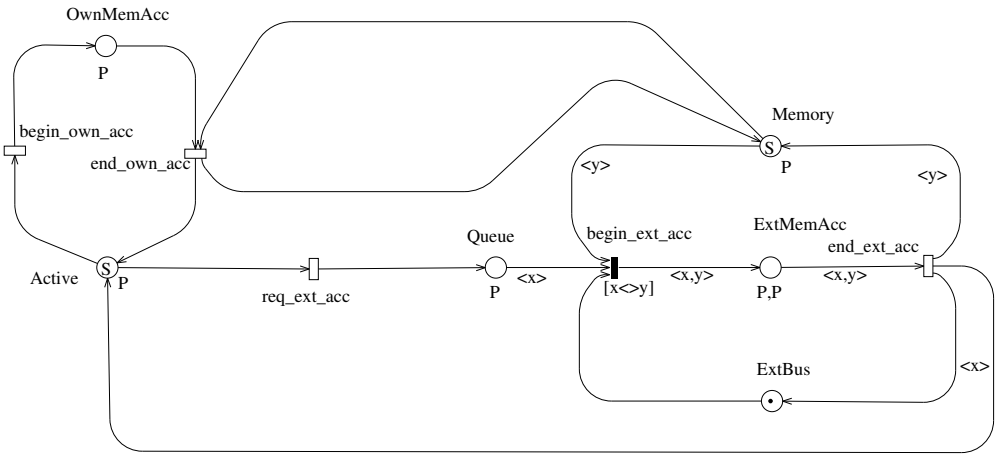

Figure 1: SWN model of a Multiprocessor architecture

The description of the system behavior requires the definition of several parameters and operating rules:

- **set of processors** P, $|P| \geq 1$;
- **activity times**;
- CM **local access times**;
- CM **remote access times**.

Our example will have a *number of processors* $|P| \geq 4$, and the *activity times*, CM *local access times* and CM *remote times* modelled by negative exponential distribution with rate λ, μ and ω respectively.

2 The description of the model

Fig.1 shows a SWN model of the multiprocessor architecture, in which the basic class P is introduced to represent the processors and their local CM identities.

The model can be decomposed in two sub-models: one representing a local CM module access, the other representing a remote CM module access for a given processor p_i. The two sub-model share the place *Memory* and *Active*·

Class id		**Description**	**Type**
P		represents the processors	unorder
Class id	**Subclass id**	**Description**	**Elements**
P	$Proc$	subclass P	p_1, p_2, p_3

Table 1: Table of Characteristics of color classes

2.1 Description of the local CM access sub-model memory

This sub-model includes transitions *begin_own_acc* and *end_own_acc* and their input/output places.

The firing of transition *begin_own_acc*, which moves a token from the place *Active* to the place *OwnMemAcc*, simulates the end of a CPU burst and the start of a local common memory access. A token of color p_i in place *OwnMemAcc* represents processor p_i accessing CM_i, if the local bus is free, or the processor p_i waiting to access CM_i, if the local bus is not free.

The firing of transition *end_own_acc* represents the conclusion of a the common memory access of processor p_i, which returns to the place *Active*.

2.2 Description of the remote CM access sub-model

This sub-model includes transition *req_ext_acc*, *begin_ext_acc* and *end_ext_acc* and all their input/output places.

The firing of transition *req_ext_acc* removing a token p_i from place *Queue* represents an external memory access request. Only if both the global bus and the local bus of the destination CM module are free the transition *begin_ext_acc* can fire, so that token p_i can move on the place *ExtMemAcc* representing the start of its external memory access.

The firing of transition *end_ext_acc* represents the end of external access for processor p_i and it moves a token p_i in place *Memory*, a token p_i in place *Active* and a neutral token in place *ExtBus*.

Place	**Description**	**Domain**
Active	Processors in active state	P
OwnMemAcc	Processors in local CM access or blocked state	P
Queue	Processors in queued state	P
ExtMemAcc	Processors accessing an extern CM module	$P \times P$
Memory	LB_i state: busy/idle	P
ExtBus	GB state: busy (no token) idle (token is presents)	*neutral*

Table 2: Table of places

Transition	Domain	Weight
$begin\_own\_acc$	P	λ
end_own_acc	P	μ
req_ext_acc	P	λ
$begin\_ext\_acc$	$P \times P$	1
end_ext_acc	$P \times P$	ω

Table 3: Table of transitions

2.3 Description of the initial state

Initial marking m_0 corresponds to the state where all processors in P are in activate state (set P in place *Active*), all local busses are idle (set P in place *Memory*) and the global is idle (one neutral token in the place *ExtBus*).

Example $|S| = 3$

Memory(1<p1>1<p2>1<p3>)ExtBus(1)

3 Number of state of SRG and RG

Table 4 shows the number of symbolic and ordinary markings (tangible / vanishing), for the multiprocessor architecture model, obtained from the SWN model in Fig.1 with only one global bus and for a variable number of processors. From an analysis of results , it is evident that the dimension of SRG is moderate even ten processors. On the contrary RG has an exponential growth as the number of processors increases. The reason is that the system behavior is symmetric.

Some performance parameters of that can be computed from the model are showed in the Table 4 too: **the CPU burst length** and **the average external accesses duration**. These Performace figures can be computed from steady state probability of symbolic markings using the following formulas:

- $E[AP] = \sum_{M \in tang(SRG)} \psi(M) \#Active$
  where $\psi(M)$ is the steady state probability of the symbolic marking M, while $\#Active$ is the number of elements in place *Active* defined as $\#Active = \sum_{<Z_1^j> \in M(Active)} card(Z_1^j)$;
- $U[GB] = \sum_{M \in tang(SRG): M(GB)=0} \psi(M)$.

Processors	**|SRG|**	**|RG|**	**|RG|/|SRG|**	**E(AP)/n**	**U(GB)**
2	6	10	1.66	0.6752411	0.27009645
3	13	62	4.76	0.6600941	0.39605642
4	23	340	14.78	0.642929	0.51434340
5	36	1652	45.88	0.6227463	0.62274684
6	52	7354	141.42	0.5991253	0.71895120
7	71	30746	433.04	0.5719982	0.80079870
8	93	122728	1391.65	0.5417373	0.86678098
9	118	472904	4007.66	0.5092124	0.91658070
10	145	1772494	12224.09	0.4756961	0.95139024

Table 4: Table of marking of multiprocessor architecture

References

[1] Giovanni Chiola, Claude Dutheillet, Giuliana Franceschinis and Serge Haddad. *Stochastic Well-Formed Colored Nets and Symmetric Modeling Application*. EEE Trans. Computer. C-42(11), Nov. 1993.