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# gaZ: group of Computer Architecture University of Zaragoza

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## Mission

**Research and train researchers in heterogeneous systems and CMPs and their memory hierarchies, focusing on general purpose computing, hard real-time or important applications such as DNA sequencing, machine learning or on-board satellite processing. Diverse teams are smarter. So gaZ promotes activities to close the gender gap in all its activities, from dissemination to research.**

## Vision

**Contribute to the design of low-power, high-performance, and reliable processors and accelerators in a open hardware environment, considering different markets, such as intelligent IOT sensors, supercomputers, mobile devices and data center servers**

## Group Profile

## Recent / Ongoing Results

### Research

- **On-chip Multicore Cache Hierarchy:** prefetching, replacement, STTRAM
- **Heterogeneous Systems** (cpu+gpu+fpga): load-balancing runtimes, accelerators
- **Real-Time systems:** static estimation of WCET, temperature-aware scheduling
- **Reliable Systems:** permanent, transient, and aging-induced fault tolerance
- **Application Acceleration**
- **Embedded Systems & IoT**

- **Architecture and Programming of High-Performance, Low-Power Scalable Computers** (TIN2016-76635-C2-1-R)
  - Joint Project with Universidad de Cantabria (2017-20)
  - New Project under evaluation
- **Gobierno de Aragon reference research group:** T58\_17R
- **TRAFAIR (2017-EU-IA-0167)**, Understanding Traffic Flow to improve Air quality, Connecting Europe Facility (CEF)



### Training/Teaching

- Digital Design
- Computer architecture & organization
- Operating Systems & Virtualization
- Networks & System administration
- Heterogeneous Systems
- RT Embedded Systems & IoT
- Data Centers

- **Computer, Telecommunication, and Industrial Engineering undergraduate and graduate programs** (including Degree and Master Final Projects)
- **PhD program with mention towards excellence**
- Several educational papers on **how to teach energy and power in computers**
- **Collaborations with other teaching areas:** building bridges across the abstraction levels of a computer system:
  - Exposing **Abstraction-Level Interactions** with a Parallel Ray Tracer. Workshop on Computer Architecture Education, 2019

### Innovation

- Application optimization
- Accelerator design
- Citizen science, dissemination of embedded systems & IoT

- **FCT-18-13586 - Make It Special** embedded systems to assist people with disabilities
- **FPGA accelerators for Machine Learning** improve the accuracy of the forecast system of *Puertos del Estado*
- **Accelerating DNA sequencing** for Intel KNL processors
- **Sending IoT into the atmosphere**
- **High-Performance, Low-Power Computer Vision for Virtual Reality** (with Eonite Inc. Palo Alto, CA, USA)



## Group positioning & Perspectives in front of Open-Hw & RISC-V

### R+D+i+T

- The RISC-V open Hw/Sw
  - Enables collaboration and can foster our regional markets
  - Is a clear educational path for Computer Architecture and Operating Systems in the undergraduate and master studies
- IA accelerators and virtualization for RISC-V cores and related application developments
- Low power RISC-V cores for IoT with non-volatile cache memories
- Use RISC-V as innovator driver-thread for universities and collaborative training strategies for all education levels

### Global Remarks

*“If many organizations design processors using the same ISA, the greater competition may drive even quicker innovation. The goal is to provide processors for chips that cost from a few cents to \$100.”*

*J. Hennessy & D. Patterson – “A New Golden Age for Computer Architecture” CACM Feb. 2019*