Bridging the Processor/Memory Performance Gap

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Device scaling in processor fabrication technologies along with micro-architectural innovation have led to a tremendous gap between processor and memory performance, also known as the memory wall. While architects have primarily relied on deeper cache hierarchies to reduce this performance gap, the limited capacity in higher cache levels and simple data placement/eviction policies have resulted in diminishing returns for modern workloads with large memory footprints and adverse memory access patterns.

This course will first describe the memory wall in modern computer systems. It will then present a spectrum of techniques that rely on prediction and speculation in hardware to enhance memory-level parallelism and hide/tolerate long memory latency.

This course assumes background knowledge on basic processor micro-architecture, memory systems and cache hierarchies.

Topics of this course are:

- The memory wall and processor-centric techniques
- Temporal streaming and address-based prefetching
- Spatial streaming and instruction-based prefetching
- Dead-block prediction and coherence speculation techniques
- Store-wait free multiprocessors and atomic store ordering

19-23 July, 2010. Timetable

Mo-19	Tu-20	We-21	Th-22	Fr-23
10:00 - 13:00 Lecture	10:00 - 13:00 Lecture	10:00 - 13:00 Lecture	9:00 - 13:00 Lab	10:00 - 13:00 Lecture
			16:00 - 20:00 Lab	

Profesor Invitado del curso “Programación Orientada a Prestaciones”
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